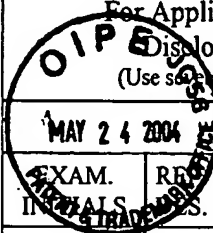
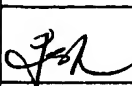
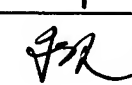


Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use separate sheets if necessary)		ATTY. DKT. NO. 5500-97900 APPLICANT: Chen, et al FILING DATE: September 4, 2003		SERIAL NO. 10/655,390 GROUP: 2825	
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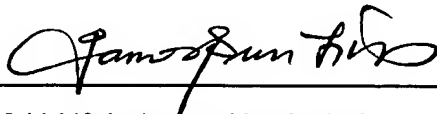


U.S. PATENT DOCUMENTS							
EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE APPROPRIATE

FOREIGN PATENT DOCUMENTS							
EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
	A1 "Wattch: A Framework for Architectural-Level Power Analysis and Optimations", Brooks, et al, ISCA, 2000, Vancouver BC Canada, 1-58113-232-8/00/6.
	A2 "An Enhanced Access and Cycle Time Model for On-Chip Caches", Wilton, et al, Western Research Laboratory, Palo Alto, CA, July, 1994.
	A3 "Evaluation of Architecture-Level Power Estimation for CMOS RISC Processors", Sato, et al, IEEE, 1995, 0-7803-3036-6/95.
	A4 "Power and Performance Simulator: ESP and its Application for 100MIPS/W Class RISC Design", Sato, et al, IEEE, 1994, 0-7803-1953-2/94
	A5 "A Technique to Determine Power-Efficient, High-Performance Superscalar Processors", Conte, et al, IEEE, 1995, 1060-3425/95
	A6 "Reducing Power in High-Performance Microprocessors", Tiwari, et al, ACM, San Diego, CA, 1998, 0-897-964-5/98/06.
	A7 "Instruction-Level Power Estimation for Embedded VLIW Cores", Sami, et al, ACM, San Diego, CA, 2000, 1-58114-268-9/00/5.
	A8 "Power Estimation of System-Level Buses for Microprocessor-Based Architectures: A Case Study", Fornaciari, et al, Proceedings of the 1999 IEEE International Conference on Computer Design, October, 1999, Austin, TX.
	A9 "System-Level Power Optimization: Techniques and Tools", Benini, et al, ACM, San Diego, CA, 1999, 1-58113-133-X/99/0008.
	A10 "Architectural Level Hierarchical Power Estimation of Control Units", Chen, et al, IEEE, 1998, 0-7803-4980-6/98.
	A11 "Microprocessor Power Estimation Using Profile-Driven Program Synthesis", Hsieh, et al, IEEE, 1998, 0278-0070/98.

EXAMINER:



DATE CONSIDERED:

9-15-05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.